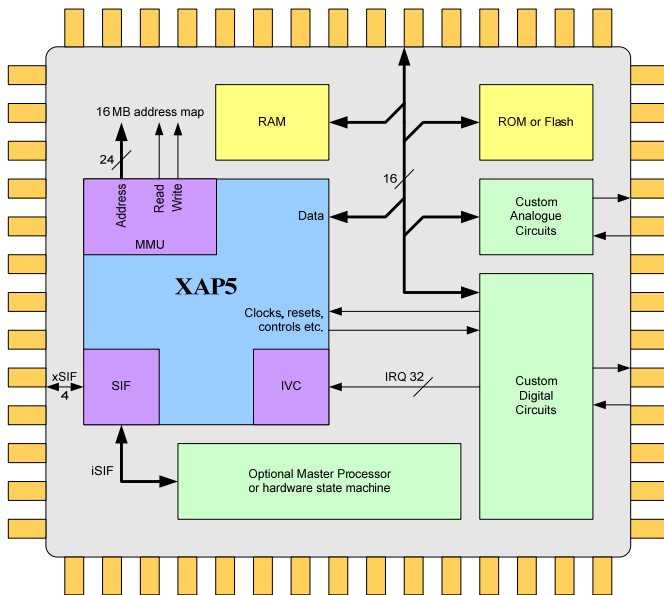


## XAP5 processor core



The XAP5 16-bit processor core targets cost-sensitive ASIC or FPGA products running sophisticated programs and requiring high performance with low power consumption. XAP5 addresses the application needs of markets such as consumer, medical devices, healthcare, automotive, industrial and wireless. It is ideal for high volume applications like Bluetooth, ZigBee, GPS, RFID and Near Field Communications.

XAP5 is a modern 16-bit RISC processor with an advanced software tool chain that efficiently manages 16 MB of memory. It is a soft IP core in Verilog RTL.

At just 18k gates XAP5 combines small size and low power with high performance. It can often replace a 32-bit core, with considerable memory cost savings.

The Cambridge Consultants XAP<sup>®</sup> family offers both 16- and 32-bit processors for a range of applications.

### XAP5a features

- 16-bit, 16 MB processor.
- Eight 16-bit registers.
- 24-bit registers: Program Counter, two Stack Pointers, Vector Pointer, four Breakpoints
- User mode and three privileged modes (Supervisor, Recovery and Interrupt).
- Powerful nested exceptions and interrupts, with response of 9 to 15 clocks.
- Von Neumann architecture with little endian organisation.
- High code density – better than leading 32-bit processors.
- 0.63 Dhrystone MIPS/MHz.
- Fast 50 DMIPS at 80 MHz.
- Small 18k gates in 0.09 mm<sup>2</sup>.
- Dynamic power of 26  $\mu$ W/MHz.
- SIF serial debug interface.
- xIDE with GCC C compiler.
- Soft core, Verilog RTL delivery.

Performance quoted on 130 nm CMOS logic

### Introduction

XAP5 is the mid-range core in Cambridge Consultants' 16- and 32-bit family of processors that offers a consistent architecture and programming environment.

XAP5 is a 16-bit RISC processor capable of efficiently managing a large 16 MB address space for programs, data and peripherals. In many applications a XAP5 could be used instead of a 32-bit processor, thus saving power, silicon area and cost. Significant additional savings result from using 16-bit wide local RAM in place of 32-bit.

The current version, XAP5a, has a two-stage pipeline that maximises processing performance at low clock speed. Combined with high code density, this can enable programs to run direct from Flash memory, saving on-chip RAM cost.

The XAP5 processor hardware includes a single-cycle 32-bit shifter, a multi-cycle multiplier (16x16) and a multi-cycle divider (32/16). Instruction fetch, decode and execution is pipelined.

### Value and performance

XAP5 is a 16-bit processor that delivers high performance for cost-efficient ASIC designs. 16-bit data offers sufficient precision for most applications and the use of 16-bit program variables can halve the number of bits of data RAM in an ASIC when compared to a 32-bit system. Using a 16-bit RAM saves power, silicon area and cost.

XAP5 features high-density program code with freely mixed 16-, 32- and 48-bit instructions that are read onto its 16-bit bus in 1, 2 or 3 clocks. The XAP5a will clock easily at 80 MHz on a 130 nm process when it gives 50 Dhrystone MIPS performance, i.e. a benchmark of 0.63 DMIPS/MHz. Or it can be clocked slowly, at say 16 MHz, when it could run programs direct from Flash memory and still deliver almost 10 MIPS performance.

XAP5 uses 24-bit addressing for program code up to 16 MB. It runs in either 'near mode', when all data is under 64 kB, or 'far mode', when data can be anywhere in the full 16 MB. C source programs are the same for either mode and they are

compiled and assembled according to the amount of data memory they need to allocate. Performance is best in near mode, where most programs are expected to operate. However, in the event far mode is required, XAP5 runs with only a small performance reduction.

The XAP5 processor has hardware to support efficient use of the 16-bit instruction space in both near and far modes, thus achieving high code density, even when 32-bit data variables are used. It also has instructions devoted to handling single bit and 8-bit data efficiently.

### Advanced architecture

XAP5's extended program and data sizes are complimented with architectural enhancements. XAP5 has eight 16-bit registers and dedicated 24-bit registers for the vector pointer, stack pointers and program counter. There are also four break point registers enabling complex debugging. XAP5 has protected operating modes for robust software operation. There is a mode for running the user's code and three privileged modes for supervisor, recovery and interrupt processing code.

XAP5's 191 instructions include multi-cycle instructions to accelerate C function entry and exit, block copy, block store, multiply and divide.

XAP5's interrupt controller gives a fast response to real-time events. Special instructions and processor hardware support nested interrupts and push and pop registers on and off the stack in the interrupt service routine. Interrupt priorities can all be assigned by software. This provides excellent interrupt entry latency of between 9 and 15 clock cycles, depending on the current instruction length.

### ASIC system design

The XAP5a is a soft IP core written in Verilog RTL intended for ASIC synthesis. Licensees can also synthesise it for verification in FPGA. The core includes an interrupt vector controller, SIF debug interface and a memory management unit that designers customise to interface with memory (Flash, ROM and RAM) and memory-mapped peripherals.

In battery operated systems the XAP5 can be synthesised for low gate count and slow clock frequency to minimise power consumption. A sleep instruction shuts down the processor until it sees a wake-up signal. The XAP5a with all its registers, the SIF and an MMU occupies less than 0.09 mm<sup>2</sup> of 130 nm silicon, i.e. around 18k gates. It consumes just 26 µW per MHz of dynamic power.

Cambridge Consultants' patented SIF interface provides a non-invasive debug facility capable of fully controlling the processor core and acquiring data from inside the processor and any memory-mapped peripheral. SIF uses a high-speed serial interface for external debug access. It also provides an internal system interface that can put the XAP5 under hardware control of a master processor or state machine.

### Programming

XAP5 can support complex software systems where high reliability and security are needed. C programs are easily and efficiently ported to XAP5 with its dynamically relocatable code and support for unaligned byte addresses minimising the code and data size in memory.

The xIDE integrated development environment provides a cross-platform program development and debugging tool for XAP5 in both near and far modes. It includes local variable debug, an instruction set simulator, a BinUtils assembler and linker and a GCC C compiler for extended ANSI C. Simulation can be extended using Python scripting to model other parts of an ASIC. XAP5 supports Real Time Operating System ports of CMX and Micrium uC/OS-II. Embedded Linux and others will follow soon. This all makes XAP5 attractive to professional programming teams.

Cambridge Consultants develops xIDE and other tools, such as its SIF non-invasive debug, which combine to reduce risk and time-scale for projects using XAP5. Designers using these tools should get their ASIC right first time, even if programs are in on-chip ROM.

ASIC application development can be accelerated by the provision of customised versions of xIDE with software plug-ins that understand the ASIC. Cambridge Consultants can supply xIDE with such plug-ins and the licensee's brand identity.

XAP		
Core	Data	Address
XAP4	16-bit	64 kB
XAP5	16-bit	16 MB
XAP3	32-bit	4 GB

Selected XAP programmers' manuals and free 30-day trial copies of xIDE for XAP processors can be downloaded from:

[www.CambridgeConsultants.com/ASIC](http://www.CambridgeConsultants.com/ASIC)

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