

## Cell No: cclasic/bravo/adc/1.0

### Delta Sigma ADC

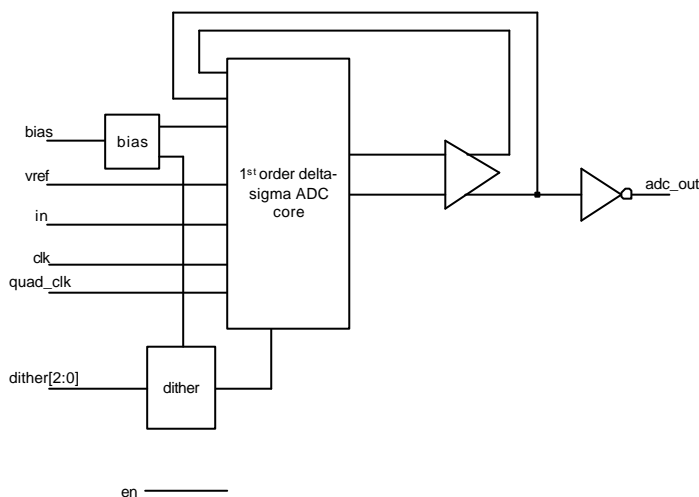
#### Cell Description

This block is a first order Delta-Sigma Analogue-to-Digital converter. The ADC generates a single bit output stream at 625 KHz. A digitally generated dither signal is supplied to break up 'idle' codes inherent in delta-sigma converters.

The advantages of this architecture are:

- Delta-sigma converter for high resolution and noise shaping
- Dither included for reduction in distortion
- Minimal amount of analogue circuitry for reduced risk/complexity
- Built-in test and de-bug facilities

#### Cell Diagram



#### Pin List

inputs	
en	Logic level enable
bias	Bias current
in	ADC input
vref	Voltage ref
dither[2:0]	dither signals
clk	Clock for ADC
quad_clk	Quadrature clock for ADC
outputs	
adc_out	Single bit ADC output
supply	
psupply	Positive supply
nsupply	Negative supply

#### Specification

parameter	value
Current Consumption	< 1.0 mA
Offset voltage	+/- 20mV
Offset drift	+/- 5mV
Full scale input	Vref +/-3%
Integral non-linearity	0.1% full scale
Start-up time	50µs

#### Technology

Process	CMOS
	double poly
	3 metal
Supply	3.3v typ (2.2v to 3.7v)